HYBRID MODE ILLUMINATION FOR FACIAL RECOGNITION AUTHENTICATION

PRIORITY CLAIM

This patent claims priority to U.S. Provisional Patent Application No. 62/730,115 to Kalscheur et al., entitled "HYBRID MODE ILLUMINATION FOR FACIAL RECOGNITION AUTHENTICATION", filed Sep. 12, 2018, which is incorporated by reference in their entirety.

BACKGROUND

1. Technical Field

Embodiments described herein relate to methods and systems for operating a facial recognition authentication process on a device. More particularly, embodiments described herein relate to operating a facial recognition authentication process using a combination of flood infrared illumination and patterned illumination of the user attempting to be authenticated by the facial recognition authentication process.

2. Description of Related Art

Facial recognition processes may be used to authenticate users for computer devices having a camera. In facial recognition processes, the user may be illuminated with illumination while images of the user are captured by the camera. In some cases, flood infrared illumination is used to assess two-dimensional information about the user being authenticated. Patterned illumination may be used in facial recognition processes to assess three-dimensional (e.g., "depth map") information about the user being authenticated. Traditionally devices may separately capture images using the different types of illumination to avoid one type of illumination affecting the other type of illumination.

SUMMARY

A user's face may be illuminated with both flood infrared illumination and patterned illumination in images captured by a device (e.g., a mobile device) to be used in a facial recognition authentication process. The flood infrared illumination and patterned illumination may be provided by a single illuminator or a combination of illuminators. Both flood infrared illumination data and depth map image data may be generated from the captured images. Flood infrared illumination data may be generated by assessing areas in the images between features (e.g., speckles) in the illuminated pattern. Depth map image data may be generated by assessing the pattern illuminated on the user's face in the images. The flood infrared illumination data and the depth map image data may be generated separately from the captured images. The facial recognition authentication process may attempt to authenticate the user in the captured images as an authorized user of the device by using the flood infrared illumination data and/or the depth map image data.

BRIEF DESCRIPTION OF THE DRAWINGS

Features and advantages of the methods and apparatus of the embodiments described in this disclosure will be more fully appreciated by reference to the following detailed description of presently preferred but nonetheless illustrative embodiments in accordance with the embodiments described in this disclosure when taken in conjunction with the accompanying drawings in which:

FIG. **1** depicts a representation of an embodiment of a device including a camera.

FIG. **2** depicts a representation of an embodiment of a camera.

FIG. **3** depicts a representation of an embodiment of a processor on a device.

FIG. **4** depicts a flowchart of an embodiment of a facial recognition authentication process.

FIG. **5** depicts a representation of an embodiment of a pair of images that includes a flood IR image and a patterned illumination image.

FIG. **6** depicts a representation of an embodiment of a series of several pairs of images.

FIG. **7** depicts a representation of an embodiment of a hybrid image.

FIG. **8** depicts a representation of an embodiment of a series of hybrid images.

FIG. **9** depicts a representation of an embodiment of a series of hybrid images with empty frames in the series.

FIG. **10** depicts a flowchart of an embodiment of an empty frame verification process.

FIG. **11** depicts a representation of an example of an embodiment of combining of hybrid images into a composite image.

FIG. **12** depicts a block diagram of one embodiment of an exemplary computer system.

FIG. **13** depicts a block diagram of one embodiment of a computer accessible storage medium.

While embodiments described in this disclosure may be susceptible to various modifications and alternative forms, specific embodiments thereof are shown by way of example in the drawings and will herein be described in detail. It should be understood, however, that the drawings and detailed description thereto are not intended to limit the embodiments to the particular form disclosed, but on the contrary, the intention is to cover all modifications, equivalents and alternatives falling within the spirit and scope of the appended claims. The headings used herein are for organizational purposes only and are not meant to be used to limit the scope of the description. As used throughout this application, the word "may" is used in a permissive sense (i.e., meaning having the potential to), rather than the mandatory sense (i.e., meaning must). Similarly, the words "include", "including", and "includes" mean including, but not limited to.

Various units, circuits, or other components may be described as "configured to" perform a task or tasks. In such contexts, "configured to" is a broad recitation of structure generally meaning "having circuitry that" performs the task or tasks during operation. As such, the unit/circuit/component can be configured to perform the task even when the unit/circuit/component is not currently on. In general, the circuitry that forms the structure corresponding to "configured to" may include hardware circuits and/or memory storing program instructions executable to implement the operation. The memory can include volatile memory such as static or dynamic random access memory and/or nonvolatile memory such as optical or magnetic disk storage, flash memory, programmable read-only memories, etc. The hardware circuits may include any combination of combinatorial logic circuitry, clocked storage devices such as flops, registers, latches, etc., finite state machines, memory such as static random access memory or embedded dynamic random access memory, custom designed circuitry, programmable logic arrays, etc. Similarly, various units/circuits/compo-